REMARKS

Claims 1-4, 7-17 and 22-30 are pending in this application, of which claims 11-17 have been withdrawn from consideration. Claims 5, 6 and 18-21 have been canceled. Claims 22-30 have been newly added. Claims 1, 2 and 4 are herein amended. Reconsideration of the rejections in view of these amendments and the following remarks is respectfully requested.

Claim Rejections – 35 USC §103

Claims 1, 2, 5 and 6 were rejected under 35 USC §103(a) as being unpatentable over Kasai et al (*W/WNx/Poly-Si Gate Technology for Future High Speed Deep Submicron CMOS LSIs*) in view of Jeng et al (U.S. Patent No. 5,877,074).

Applicants respectfully traverse this rejection.

In the Office Action the Examiner alleged as follows:

> In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., the impurity incorporated in the poly crystalline silicon films) are not recited in the rejected claims. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims.
>
> The main issue here is whether or not the second polycrystalline silicon film of Kasai, in view of Jeng '074, having the thickness as claimed (2-20 nm). . . . .

(Citation omitted).

In view of the Examiner's allegation, claim 1 has been amended to recite, among other things, "a gate electrode formed above the silicon substrate between the pair of impurity diffused regions with a gate insulation film interposed therebetween, the gate electrode being formed of a first polycrystalline silicon film formed on the gate insulation film and doped with boron, a

second polycrystalline silicon film formed on the first polycrystalline silicon film having a thickness ~~of 2-20 nm and~~ thinner than that of the first polycrystalline silicon film and having crystal grain boundaries which are discontinuous to the first polycrystalline silicon film, and a metal nitride film formed on the second polycrystalline silicon film, the second polycrystalline silicon film being for preventing boron in the first polycrystalline silicon film from diffusing toward the metal nitride film." This amendment is supported in the specification, e.g., page 7, lines 6-14.

Thus, claim 1 recites that first polycrystalline silicon film is doped with boron and that the second polycrystalline silicon film is formed between the first polycrystalline silicon film and the metal nitride film in order to prevent boron in the first polycrystalline silicon film from diffusing toward the metal nitride film. According to this feature of claim 1, decrease of the boron concentration in the first polycrystalline silicon film is suppressed, thus the depletion of the gate electrode which affects characteristics of the MOS transistor can be prevented.

In Jeng et al, the non-doped amorphous silicon film 32 is formed between the doped polycrystalline silicon film 31 and the tungsten silicide film 14 in order to prevent the diffusion of the fluorine introduced from WF_6 gas during the deposition of the tungsten silicide film 14. Thus, the amorphous silicon film 32 of Jeng et al is clearly different from the second polycrystalline silicon film of claim 1.

The MOS transistor of Jeng et al has so-called polycide gate structure, so that the gate electrode has no metal nitride film. In Jeng et al, the amorphous silicon film 31 is doped with not boron but phosphorus. Thus, Jeng et al neither teaches not suggests the prevention of boron diffusion toward the metal nitride film.

Jeng et al discloses in column 1, lines 48-53 that the metal nitride film has a function to prevent fluorine atoms from diffusing into the gate polycrystalline silicon layer. Thus, in Kasai et al., it is not necessary for considering the fluorine diffusion, because the gate electrode of Kasai et al has a metal nitride film formed between the polycrystalline silicon film and the tungsten film. Therefore, one of ordinary skill in the art would not set the thickness of the amorphous silicon film of Kasai et al to the thickness of the amorphous silicon film 32 of Jeng et al based on Jeng et al.

For at least these reasons, claim 1 patentably distinguishes over Kasai et al and Jeng et al.

Claim 2 has been amended to recite "a gate electrode formed above the silicon substrate between the pair of impurity diffused regions with a gate insulation film interposed therebetween, the gate electrode being formed of a first polycrystalline silicon film formed on the gate insulation film and doped with boron as a first impurity and with a second impurity other than boron, a silicon oxide film formed on the first polycrystalline silicon film, a second polycrystalline silicon film formed on the ~~first polycrystalline~~ silicon oxide film having a thickness ~~of 2-20 nm and~~ thinner than that of the first polycrystalline silicon film and having crystal grain boundaries which are discontinuous to the first polycrystalline silicon film, and a metal nitride film formed on the second polycrystalline silicon film~~, and a metal film form on the metal nitride film~~."

The amendment of claim 2 is supported in the specification, e.g., page 27, line 21 to page 28, line 16. Examples of the second impurity are described in, e.g., page 31, lines 13-22. The second feature of the amendment of claim 2 is described in, e.g., page 29, lines 5-9 of the specification of the present application.

Thus, claim 2 recites that the first polycrystalline silicon film formed on the gate insulation film is doped with boron as a first impurity and with a second impurity other than boron. As the second impurity, an impurity which can amorphize the surface of the polycrystalline silicon film by ion implantation, for example, is applicable.

In Kasai et al, the amorphous silicon film is doped with boron or phosphorus. Kasai et al neither teaches nor suggests that the amorphous silicon film is doped with the two kinds of impurities. Thus, Kasai et al is different from the present invention and does not provide any motivation for the present invention.

In Jeng et al, the amorphous silicon film 31 is doped with phosphorus. Jeng et al neither teaches nor suggests that the amorphous silicon film is doped with the two kinds of impurities. Thus, Jeng et al is clearly different from the present invention and does not provide any motivation for the present invention.

For at least these reasons, claim 2 patentably distinguishes over Kasai et al and Jeng et al.

Claims 3, 4 and 7-10 were rejected under 35 USC §103(a) as being unpatentable over Kasai et al in view of Jeng et al, and further in view of Tsukamoto (U.S. Publication No. 2001/0000629).

Claims 3, 4 and 7-10 depend from claim 1 or 2. As described above, claims 1 and 2 patentably distinguish over Kasai et al and Jeng et al.

Tsukamoto was cited for allegedly disclosing that a native oxide film (20) is formed between the first (6) and second (7) polycrystalline silicon film so that the grain size of the second polycrystalline silicon film (7) can become large. Such disclosure, however, does not remedy the deficiencies of Kasai et al and Jeng et al.

For at least these reasons, claims 3, 4 and 7-10 patentably distinguish over Kasai et al in view of Jeng et al, and further in view of Tsukamoto.

New Claims

Newly added claim 24 is the same as the original claim 1 except that it recites the thickness of the second polycrystalline silicon film. Claim 24 recites that the second polycrystalline silicon film has a thickness of 2-10 nm. This is supported by the specification describing embodiments of the present invention showing the thickness of the second polycrystalline silicon film set to 10 nm (see, e.g., page 23, lines 20-22 of the specification of the present application).

As described in page 8, line 26 to page 9, line 9 of the specification of the present application, when the second polycrystalline silicon film is too thick, the contact resistance between the first polycrystalline silicon film and the metal nitride film increases and the etching for forming the gate electrode may be complicated. Thus, the above-described thickness range of the second polycrystalline silicon film is based on the disclosure of the present application, so that claim 24 would not raise the issue of new matter.

Claim 24 has a feature that the second polycrystalline silicon film has a thickness of 2-10 nm. According to this feature of the present invention, the impurity diffusion from the first polycrystalline silicon film to the metal nitride film formed on the second polycrystalline silicon film can be suppressed without increasing the contact resistance.

In Kasai et al, the thickness of the amorphous silicon film is set to 100 nm (see page 19.4.1, right column, lines 17-20). Kasai et al neither teaches nor suggests the 2-10 nm-thick amorphous silicon film. Thus, Kasai et al is clearly different from the present invention and does not provide any motivation for the present invention.

In Jeng et al, the thickness of the amorphous silicon film 32 is set to 20-40 nm (see column 3, lines 11-13). Jeng et al neither teaches not suggests the 2-10 nm-thick amorphous silicon film. Thus, Jeng et al is clearly different from the present invention and does not provide any motivation for the present invention.

In Tsukamoto, the thickness of the amorphous silicon film 7 is set to 70 nm (see paragraph [0064]). Tsukamoto neither teaches nor suggests the 2-10 nm-thick amorphous silicon film. Thus, Tsukamoto is clearly different from the present invention and does not provide any motivation for the present invention.

For at least these reasons, claim 24 and its dependent claims 25-30 patentably distinguish over Kasai et al, Jeng et al and Tsukamoto.

If the Examiner believes that this application is not now in condition for allowance, the Examiner is requested to contact the undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees that may be due with respect to this paper to Deposit Account No. 50-2866.

Respectfully Submitted,

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